High Density Interconnect Multi-Chip Module for the Front-End Electronics of the PHENIX/MVD

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Abstract

A multi-chip module (MCM) based on High Density Interconnect (HDI) technology was developed for the front-end electronics of a high energy nuclear physics experiment to process charge pulses from silicon detectors. Stringent requirements in performance as well as low radiation length and minimum physical size of the module dictated the use of the most sophisticated MCM technology available. The module handles 256 input channels on an alumina substrate with milled cavities for die placements and four layers of thin-film traces of 42u width. A total of 20 custom integrated circuit chips and 98 passive components are assembled on a substrate of size 43mm x 48mm. Various aspects of development efforts for the design and fabrication as well as the electrical test results of the module are discussed.

I. INTRODUCTION

The Multiplicity Vertex Detector (MVD) is a subsystem of the PHENIX physics detector for the RHIC accelerator, Brookhaven National Laboratory. The main function of the MVD is to determine the collision vertex as well as the multiplicity of the collision-induced charged particles. It has 34,720 signal channels (on 136 MCMs total) from both silicon strip and pad detectors to process signals from ionizing particles at the beam-crossing rate of 9.4 MHz.

For every channel and for every beam crossing, the MVD front-end electronics captures and stores the charge amplitude in a depth of analog memory locations. Per external command called Level-1 trigger, it digitizes and reads out the contents of specific analog memory locations for post processing in the counting house.

High operational speed and complex functions in a tight volume as well as minimum radiation length required sophisticated custom electronics and highly advanced packaging, leading to the selection of the HDI-MCM. As a patented fabrication process by Lockheed-Martin GES Moorestown, NJ, HDI fabrication process starts with a thin alumina substrate, which is milled to create cavities according to the die-measurement data. Bare dice are then dropped into the cavities with the bond-pads up, showing co-planar top surfaces.

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A polyimide film is bonded over the chips to form the first dielectric layer. Then, a computer-guided laser is used to drill via holes directly to the die pads. The same laser system also patterns the metal traces for the interconnections. Multiple layers are sequentially added to form a complete MCM. Four layers were used for this MCM.

Some advantages of the HDI technology include: elimination of the need for wirebonds or solder bumps, well controlled impedances for traces for wide signal bandwidths, no mask sets for lithography, and good thermal conductivity from the chips to the substrate, all contributing to maximize the performance of the module at competitive cost.

II. DESIGN AND DEVELOPMENT OF THE MCM

A. Circuit Designs

A simplified block diagram of the MCM is shown below.

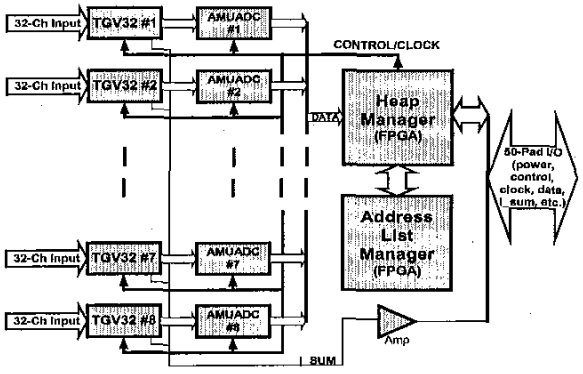

Figure 1: Top level MCM block diagram.

Each MCM carries eight pairs of 32-channel preamp-discriminator (TGV32) [1], [2], and Analog Memory Unit-ADC (AMUADC) [3] chips. Both of these custom ASICs were developed at Oak Ridge National Laboratory. Details of these chips are available in the references, but a brief description is given below.

Inside the TGV32, each electronic channel converts the charge pulses from the silicon detector into equivalent voltage steps and send it to AMUADC. Also, for those pulse steps

above threshold amplitudes, each discriminator injects a current pulse of fixed amplitude into a common current-summing node. The current-sum signal is buffered and sent to an outside data collection interface module for analog measurement of the number of channels triggered (multiplicity) per beam crossing.

AMUADC chips sample and store the TGV output waveforms at beam clock rate and, when commanded, convert two adjacent locations (before and after the beam crossing) of analog memory contents into digital data for readout. Two FPGAs (XC4010E by Xilinx) are used on the MCM for timing, control, and data formatting (for readout) either in a raw or correlated mode. The MCM also has a pass-through for the silicon detector bias supply.

B. Layout Designs

A Mentor hybrid layout tool (HybridStation) was used at the Los Alamos National Laboratory for the MCM. The design rules as supplied by the Lockheed-Martin GES was followed except where the minimum pad spacing rules were not met for the 256-channel I/O pads of TV32s and AMUADC chips. Those pads had 96-micron pitch, less than the recommended 114 microns. Close communications with foundry was necessary to ensure reliable via connections to the pads. For those pads, elongated via pads were used with offset via hole locations to maintain minimum distances between adjacent holes. Normal interconnection trace density is 42- micron widths and 42-micron spacing.

As an aid in process quality assurance, a test pattern was included on each layer. The pattern includes approximately 6mm long serpentine trace pair with minimum trace widths and separation as well as a set of vias. These patterns are tested for every metal layer and layers below it for shorts or opens and the quality of vias. In addition, eight test points were brought out to the top layer for direct measurements of signals for diagnostics purposes.

Three distinct power and returns were maintained for two different analogs and one digital supply lines. The substrate contact, at the lowest potential, laid out in the die placement cavities, is used as power return as well. All by-pass capacitors, clock terminating resistors and bias components for the current-sum buffer amplifier are surface-mounted.

C. Known-Good-Die Issues

Cost of repairing a failed MCM is high and not cost effective. All necessary precautions should be taken to ensure that the chips used in the fabrication of the MCM are tested to be known-good-dice (KGD) for high initial yield. All of the dice used in this MCM were fully tested at operating frequency prior to installation. Temperature testing was not done as the MCMs are to be operated in an actively controlled temperature environment.

For the custom ASICs, after the chips were produced at a foundry, they were shipped directly to a wafer probing and testing house, where they were tested according to the instructions and test vectors supplied. FPGAs were procured as tested units.

All passive components are surface mounted with conductive epoxy with low temperature (<85 degrees C) cure so as to minimize the thermal stress to the MCM. Since custom ASIC chip fabrication and the MCM layout were progressing almost simultaneously, the die dimensions for the TGV32s and AMUADCs were carefully controlled by adjusting the scribe lane widths for dicing.

D. MCM Fabrication

Before the MCM design was committed for fabrication, a printed circuit version of the same circuit was produced and tested for connectivity and design confirmation. Other than noise and operational clock speed, the printed circuit version worked with no interconnection change at all. The layout design data set is sent electronically to the foundry where additional verification checks were performed against design rules prior to production commitment. Close contact with the foundry was maintained at every stage of the production processes for best results. Figure 2 shows an MCM with 50-pad I/O connector cable attached. Its relative size is shown in contrast to a US 25-cent coin. Silicon strip or pad detector is connected (bond-wired) on the left edge of the MCM for signal inputs.

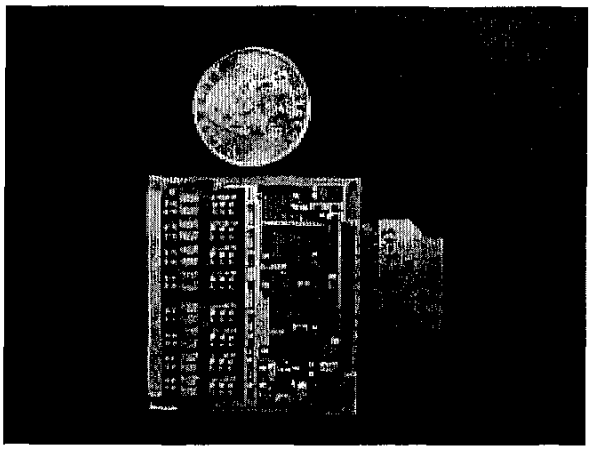

Figure 2: MCM with a flexible I/O cable attached.

III. Test Setup and Results

A. Test Setup

A test setup with the motherboard on the vertical plane of the test stand and a daughter card with an MCM on the top surface is pictured in Figure 3. The picture also shows silicon strip detector attached to the MCM through a flexible cable. Temporary aluminum heat-sink, doubling its role as a shielding ground, is used during the test, but was removed for picture clarity. In a normal operational setup, six MCMs are plugged into a daughter board which, in turn, is connected to the motherboard along with five other daughter cards. External supply of power, control and data readout are done through connectors on the motherboard.

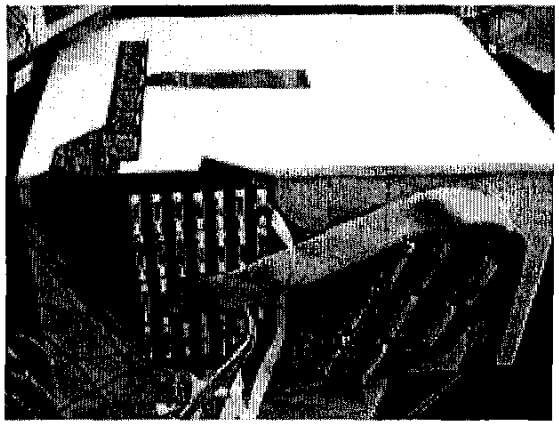

Figure 3: Test stand with a motherboard, daughter card and an MCM with a silicon strip detector.

B. *Test Results*

There were some initial start-up difficulties such as mounting tantalum capacitors with reversed polarity, balky FPGA codes, etc., all of which were eventually worked out. Initial batch of 18 MCMs was tested completely at the time of this write-up. Four of the MCMs was tested perfectly functional. Overall, approximately half of the MCMs were tested usable (having only minor defects) while the rest of the MCMs showed varying degrees of failures making those unusable. Preliminary testing of the second batch of eight (8) gave higher yield than the first at >60%.

Majority of the rejected MCMs show a number of 32-channel blocks returning useless data. Exhaustive testing and investigations indicate that such failures are most likely due to open circuits (probably an open via connection) in one of the bussed control lines that span eight AMUADCs. Another more significant symptom is in serial control bit down-loading, in which the serial bits are lost in the chain, unable to setup the chip configuration. This symptom can also be attributed to open connections as well.

A typical test sequence starts with downloading program codes for the two FPGAs through a serial link. After the FPGA code download, configuration bits for all TGV32, AMUADC and the FPGAs are sent through the same serial link. The power supply currents change with the downloads as the chips are being activated. A LabVIEW-based automated test software was developed for downloading codes and configuration bits, calibration pulse generation, and data readout/analysis.

With careful layout for reduced interference and compact dimension that resulted in minimal input capacitance, the preamplifiers exhibit a very low-noise operation. The noise was measured as a fluctuation in correlated readout data (from 10-bit ADCs), which represent noise performance as a signal chain, not just the preamplifier. Reference sensitivity of the preamplifiers was established by external charge injection using micro probes to access the input nodes.

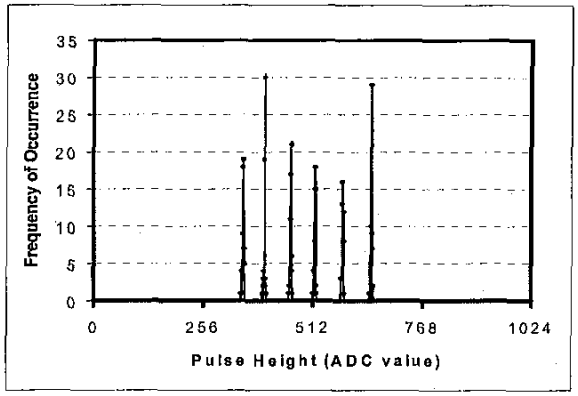

Figure 4: Typical channel response to a series of calibration pulses.

In Figure 4, a typical response of a channel to a series of calibration injections at six different amplitudes is given. X-axis is the ADC readout of the channel (proportional to the calibration pulse amplitude, ideally) while y-axis is the frequency of occurrence at the amplitude. The narrowness of the distribution determines the noise performance. Measurements show an excellent Equivalent Noise Charge (ENC) of 600 electrons RMS (see Table 1) when operated alone without the silicon detector.

Table 1
Equivalent Noise Charge (ENC) of the TGV32 preamplifier

	ENC (electrons, RMS)
MCM alone	600
With Si-Strip detector (C_{in}<24pF, I_{leak}< 50nA/ch, R_{bias}= 10M-ohm, nom)	2200

When the silicon detector is attached to the input of the MCM through a flex cable of about 10cm in length, the noise was still at a respectful 2200 electrons RMS in ENC; a signal-to-noise ratio better than 10 to 1. With such noise margin, it is clear that discriminator threshold settings of a small fraction of a mip is easily achievable. The sensitivity of the preamplifier drops with the attachment of the silicon by approximately 25%, from ~80mV/mip to ~60mV/mip.

One of the key functions of the MCM is to generate discriminator current-sum pulses of amplitudes proportional to the number of channels triggered on each beam crossing. Fine adjustments of discriminator thresholds and bias settings combined with varying amounts of charge injection were necessary to determine the characteristics of the responses.

Initial current-sum waveforms, while functional, showed an extraneous trigger from an interference source related to the

comparator reset inside the AMUADC prior to ADC actions. For the very first batch, we also discovered that a by-pass capacitor for the current-sum discriminator circuit was grounded to a wrong node, introducing interference from the AMUADC comparator switching noise.

Data conversion, formatting and readout take about 45 microseconds. The data packet is stored and displayed automatically for inspection and analysis. Many different tests are performed to verify the full functionality of the MCMs, but the more important tests include statistical measurements of noise as mentioned above and the linearity of each channel to calibration charge injections. A typical linearity measurement of the MCM to cal injection is show in Figure 5.

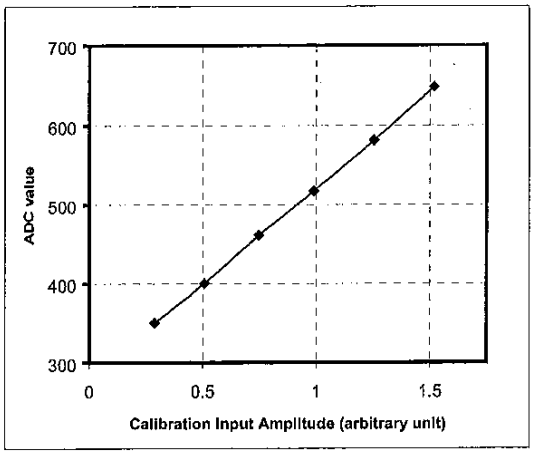

Figure 5: Linearity of a typical channel.

C. *Specifications*

Some of the more interesting specifications are given in the Table 2 below.

IV. CONCLUSIONS

Development of the MCM required careful planning, design/verification, close communication between all personnel involved, and exhaustive testing. Difficulties encountered in developing the MCM include working out the design rule infringements, foundry process glitches that delayed delivery schedules, and controlling the interference on the current-sum signals. As usual, perfecting the firmware for FPGAs took some time also. In the end, without any redesign, the MCMs performed with very good results. At the time of this writing, the only concern is on the discriminator current-sum performance, which is the key to one of the main functions of the MVD. Further deliveries and tests of the MCMs will help determine final yields and costs of producing the MCMs.

Table 2

Major specifications of the MCM

Dimension	43mm x 48mm x 1.5mm
Weight	12.9g
Power consumption, average (0.2Ax5VD, 0.13Ax 5Vanalog, 0.04A at -5V)	1.85W
Number of Channels	256
Equivalent Noise (electrons, RMS)	600 w/o detector 2200 w/detector
Number of I/O lines for power, control, clock and data interface	50
Operating clock (Beam Clock)	9.4MHz
Data Readout Clock	4x 9.4MHz

V. ACKNOWLEDGMENTS

Many people contributed to make this effort successful. Mr. Gary Richardson, now retired from the Los Alamos National Laboratory, was responsible for the difficult job of laying out the MCM with more than 1200 interconnection nodes and numerous constraints to deal with. Mr. Tony Moore of Oak Ridge National Laboratory worked hard to make sure that the TGV32 chips are all tested properly as known-good-dice.

VI. REFERENCES

[1] C. L. Britton, Jr., et al., TGV32: A 32-Channel Preamplifier Chip for the Multiplicity Vertex Detector at PHENIX", *Review of Scientific Instruments*, Vol. 70, No. 3, pp. 1684-1687, March 1999.

[2] C. L. Britton, Jr. et al., "Design and Performance of Beam Test Electronics for the PHENIX Multiplicity Vertex Detector", *IEEE Trans. Nucl. Sci.*, Vol. 44, No. 3, pp.283-288, June 1997

[3] M. S. Emery, et al., "A Multi-Channel ADC for Use in the PHENIX Detector", *IEEE Trans. Nucl. Sci.*, Vol. 44, No. 3, pp.374-378, June 1997